ANALYSIS OF TWO-STAGE SHUNT CAPACITOR BANK PROTECTION

DEFICIENCIES WITH MITIGATION SUGGESTED

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ABSTRACT

A large utility was experiencing a problem when switching a two-stage capacitor bank resulting in misoperations of the bank protection. When the bypass switch is opened a long duration dc offset occurs across all capacitors. This dc causes saturation of the tap point VT resulting in a false differential voltage and misoperation of the protection. The utility had to disable the voltage differential during switching until the phenomenon could be studied and a suitable solution found.

The work is a comprehensive analysis of the transients affecting the protection and how the problem could be mitigated.

An analytical approach was taken to understand the occurrence of the dc offset and an Electromagnetics Transients Program (EMTP) was used to study various mitigation techniques. A simple solution is presented for future installations that prevents the problem completely. A “next best” mitigation is presented for existing banks where reconfiguration would not be cost justified.
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LIST OF ABBREVIATIONS

ATP, Alternative Transients Program

EMTP, Electromagnetics Transients Program

IEEE, The Institute of Electrical and Electronics Engineers

RMS, root-mean-square

VT, voltage transformer
CHAPTER 1
INTRODUCTION

Shunt capacitor banks are widely used in utility systems to provide local reactive power and support system voltage. The voltage rise that occurs when a capacitor bank is switched on depends on the capacitive reactance ($X_C$) of the bank and the Thevenin’ impedance of the system prior to switching the capacitor bank in service as well as bus load. The system shown in Figure 1.1 can be used to calculate the resulting voltage rise by simple application of voltage division after the switch is closed to energize the capacitor bank.

Prior to closing the switch there is no current flow (neglecting load) so the bus voltage equals the system voltage. After the switch is closed we can apply voltage division,
\[ V_{BUS} = V_{SYSTEM} \frac{X_C}{X_C + Z_{THEV}} \]

Dividing the bus voltage after switch closure by the bus voltage prior to switch closure we get,

\[ V_{RISE} = \frac{X_C}{X_C + Z_{THEV}} \quad \text{(per unit)} \]

which can be simplified to,

\[ V_{RISE} = \frac{1}{1 + \frac{Z_{THEV}}{X_C}} \quad \text{(per unit)} \]

To arrive at a simple estimation of the percent voltage rise that occurs when the capacitor bank is energized we can subtract unity (assumes 1.0 per unit voltage prior) from the above equation and multiply by 100%.

\[
\%V_{RISE} = \left[ \frac{1}{1 + \frac{Z_{THEV}}{X_C}} - 1 \right] \times 100\%
\]

This simplifies further to,

\[
\%V_{RISE} = \left[ -\frac{Z_{THEV}}{X_C} \right] \times 100\%
\]

When \( Z_{THEV} \ll X_C \) this reduces to,

\[
\%V_{RISE} \approx -\frac{Z_{THEV}}{X_C} \times 100\%
\]

When \( Z_{THEV} \) is predominately inductive,

\[
\%V_{RISE} \approx \left| \frac{Z_{THEV}}{X_C} \right| \times 100\%
\]
It can readily be seen from the above equation for percent voltage rise that on weaker systems the percent voltage rise for a given capacitor bank will be higher when compared to the application of the same capacitive reactance on a strong system. As such, in weaker parts of the power system it is commonly required to segment the shunt capacitor banks into many smaller banks to allow for more incremental changes in voltage. This is often a disadvantage in urban areas or other locations where real estate is at a premium because more banks requires more space.

As early as 1953 a reconnection scheme has been suggested as a practical method to take advantage of the temporary overvoltage capability of capacitors to increase the granularity of reactive power switched [1]. In 1955 the multi-stage scheme that is being used presently was suggested as a means to reduce the step size of capacitive reactance and also benefit from the space saving feature of the design where physical space is limited [2]. The first practical applications of this multi-staged approach at transmission voltages were implemented by the Bonneville Power Authority (BPA) in the late 1990’s [3].

The first goal of this work is to show a deficiency affecting the protection of a 2-stage capacitor bank with both transient analysis using the Alternative Transients Program (ATP) and analytical solutions. The second goal is to investigate various methods to mitigate the deficiency and to improve the state of the art of capacitor bank protection.
CHAPTER 2
SCHEME EXPLANATION

General Concept of 2-Stage Capacitor Bank

Figure 2.1 shows the simplified one-line diagram for an existing 2-stage capacitor bank applied on a 161kV transmission bus. During normal operation both capacitor stages (C₁ and C₂) are energized in series. In the analysis presented in this document they are sized such that C₁ equals C₂ and both stages will share the bus voltage equally (although this is not a requirement).

Figure 2.1 One-line of two-stage capacitor bank

C₁ is comprised of four parallel strings with each string being comprised of three series capacitors rated 500 kvar and 15,920 volts. C₂ is comprised of eight parallel strings with each string being comprised of five series capacitors rated 600 kvar and 19,100 volts. A group of
three parallel low-voltage capacitors are placed on the neutral end of the bank to develop a voltage drop to present to the bank protection relays. This is detailed in Figure 2.2.

Each capacitor can in the C₁ group has a capacitive reactance of,

\[ X_{C_{500}} = \frac{15,920^2}{500,000} = 506.89\Omega \]

resulting in an overall capacitive reactance for bank C₁ of 380.17Ω. This results in a capacitance value for C₁ of 6.98μF. C₂ is computed similarly and has a capacitance value of 6.98μF. The low-voltage capacitors on the neutral end of the bank are each rated 167 kvar and 825 volts. Three in parallel equate to a capacitance of 1952μF. The resistor shown in series with the voltage transformer is purportedly used for ferroresonance suppression and is 100Ω. The voltage transformer is for galvanic isolation and has a ratio of 3.2 to 1.

When the bypass switch is open the total bank reactive power (assuming a nominal 161kV bus voltage) will be,

\[ \text{MVAR}_3 = \frac{161,000^2}{X_c} = 2\pi \cdot 60 \cdot \frac{6.98\mu F}{2} \cdot 161,000^2 = 34 \]

and when the bypass switch is closed the total bank reactive power (assuming a nominal 161kV bus voltage) will be,

\[ \text{MVAR}_3 = \frac{161,000^2}{X_c} = 2\pi \cdot 60 \cdot 6.98\mu F \cdot 161,000^2 = 68 \]
Figure 2.2 Detailed one-line of two-stage capacitor bank

Neglecting the small influence of the low-voltage capacitors, with the bypass switch open the voltage across C\textsubscript{1} and C\textsubscript{2} will be 50\% of the bus voltage or,

\[ V = 0.50 \cdot \frac{161,000}{\sqrt{3}} = 46,477 \text{V} \]

C\textsubscript{1} is rated for 3 times 15,920V for 47,760V. As such, during operation with the bypass switch open the voltage across the C\textsubscript{1} stage is 97.3\% of rated. Similarly, C\textsubscript{2} is rated for 5 times...
19,100V for 95,500V. During operation with the bypass switch open the voltage across the $C_2$ stage is 48.7% of rated.

With the bypass switch closed $C_1$ is effectively shorted out leaving $C_2$ to experience the entire bus voltage or 92,953V phase-to-ground. This equates to 97.3% of rated. This presents an added operational flexibility for this design over the design described in [3] in that neither operating mode (bypassed or un-bypassed) stresses the energized capacitors beyond their rated voltage. As such they can remain energized indefinitely as system requirements dictate. The implementation described in [3] is the same configuration except that the lower capacitor bank doesn’t have a high enough voltage rating to allow continuous operation when the upper bank is bypassed. It takes advantage of the short-term overvoltage capability of capacitors and is only intended to be used for short periods of time to improve stability during low-voltage emergencies. It is not intended for continuous operation with the upper bank bypassed.
CHAPTER 3
PROTECTION

Voltage Differential

The primary protection applied to the capacitor bank is a voltage differential scheme. This scheme is implemented substantially the same regardless of the bank design being fused or fuseless [4]. Since fuseless has become the industry norm it will be the focus in this document. Figure 3.1 is a simplified one-line of the two capacitor stages and the low-voltage capacitance used to develop voltage for the differential scheme. This is clearly a simple voltage divider circuit and the voltage across each of the capacitances will be directly proportional to the applied system voltage (1-phase) and the reactance of the capacitors.

Figure 3.1 Simplified one-line.
The voltage differential protection compares the bus voltage (1-phase) with the voltage measured across the low-voltage capacitor according to the following formula where $V_X$ is typically the bus voltage and $V_Y$ is the voltage measured at the tap point (across the low-voltage capacitance).

$$\Delta V = V_X - kV_Y$$

The constant $k$ is simply a scaling factor to balance the equation under normal conditions. The $k$ factor is set after the relay has been placed in service to “null” the above equation. Modern capacitors manufactured after 2002 in compliance with [5] “shall not vary more than -0% to +10% of their nominal value based on rated kvar, voltage, and frequency”. Older capacitors may have tolerances as high as -0% to +15%. As such, due to normal manufacturing tolerances and measurement error there will be a measurable $\Delta V$ when the bank is in service even though no capacitor elements have failed. To improve the sensitivity of the protection this unbalance is nulled with the $k$ factor. For some digital voltage differential relays this nulling is done manually when connected to the relay with a computer by prompting the relay to run a routine to determine $k$ on a per-phase basis. It is noteworthy to mention that with capacitor banks oriented in an east-west arrangement that a portion of the bank will heat up and later cool down before the rest of the bank as the sun makes its progress across the day. This causes a drift in the capacitance values because of expansion. Due to the sensitivity of the voltage differential schemes this may result in erroneous alarms as the capacitance value of the capacitors is affected by their temperature (warmer capacitors experiencing more expansion). More modern digital relays can automatically calculate the $k$ factor at various intervals as long as the voltage
difference they measure is noted to be a smooth change (due to unequal heating of the
capacitors) and not a sudden change as experienced when a capacitor element has failed.

Prior to placing the capacitor bank protection in service initial values of the $k$ factors
can be calculated as shown below for the case of the bypass switch (Figure 3.1) open. $V_X$ is the
secondary value of the bus voltage presented to the relay through a 1400:1 bus VT. $V_Y$ is the
secondary value of the tap point voltage presented to the relay through a 3.2:1 VT.

\[
V_{BUS}^{\phi} = \frac{161000}{\sqrt{3}} = 92953.4\text{V}
\]

\[
V_X = \frac{V_{BUS}^{\phi}}{1400} = 66.4\text{V}
\]

Neglecting the small impedance of the LV capacitors we can calculate the current flowing in one
phase of the capacitor bank as,

\[
I_{\phi} = \frac{V_{BUS}^{\phi}}{X_{C1} + X_{C2}} = \frac{V_{BUS}^{\phi}}{j380.2\Omega + j380.2\Omega} = -j22.2\text{A}
\]

and the voltage drop across the LV capacitance will be,

\[
V_{TAP} = I_{\phi} \cdot X_{LV} = \frac{I_{\phi}}{2\pi \cdot 60 \cdot 1952.5\mu F} = 521.7\text{V}
\]

with the resulting voltage to the relay (normally negligible drop in the 100Ω resistor) being,

\[
V_Y = \frac{V_{TAP}}{3.2} = 163.0\text{V}
\]

Now the initial $k$ factor can be calculated as,

\[
k = \frac{V_X}{V_Y} = \frac{66.4\text{V}}{164.0\text{V}} = 0.4
\]
Voltage Settings

To determine the voltage differential settings failures in the upper bank ($C_1$) will be examined and then failures in the lower bank ($C_2$). The goal of the voltage differential will be to trip the bank when the voltage across any capacitor element exceeds 110% of rated voltage. Note also that two different settings are required depending on the bypass switch being closed or open. Figure 3.2 shows the internal connections of the individual capacitor elements for both the 500kVAR and 600kVAR units used in this installation. The 500kVAR capacitor units are comprised of eight (8) series connections of two (2) capacitor elements in parallel. The 600kVAR capacitor units are comprised of ten (10) series connections of two (2) capacitor elements in parallel.

The failure mode of all-film fuseless capacitors is to fail shorted producing a stable “weld” across several layers between two electrodes [4]. When this occurs it produces an overvoltage on the remaining elements in the capacitor unit and bank. Usually the electrodes are aluminum foil and the dielectric film is polypropylene.
The calculations of the capacitive reactance of the 500kVAR capacitor unit and the 600kVAR capacitor unit are repeated below.

\[
X_{c500} = \frac{15,920^2}{500,000} = 506.9\Omega \\
X_{c600} = \frac{19,100^2}{600,000} = 608.0\Omega
\]

With no failures the upper bank capacitive reactance will be,

\[
X_{c1} = \frac{3}{4} \cdot \frac{15,920^2}{500,000} = 380.2\Omega
\]

and the lower bank capacitive reactance will be,

\[
X_{c2} = \frac{5}{8} \cdot \frac{19,100^2}{600,000} = 380.0\Omega
\]

When an individual element shorts out it will short out its series group inside the capacitor unit. In the case of a 500kVAR capacitor unit this will result in a decrease in the capacitive reactance...
of the upper bank \((C_1)\) by a factor of \(7/8\) since these units have eight (8) series groups. The resulting capacitive reactance of the capacitor unit with one (1) shorted element is calculated below and a prime mark has been used to distinguish it from the healthy reactance for a 500kVAR unit.

\[
XC'_{500} = \frac{7}{8} \cdot \frac{15,920^2}{500,000} = 443.5 \Omega
\]

Referring to Figure 2.2 we see that the upper bank \((C_1)\) is comprised of four (4) strings of three (3) capacitor units in series. The capacitive reactance of a healthy string is,

\[
X_{STRING} = 3 \cdot \frac{15,920^2}{500,000} = 1,520.7 \Omega
\]

and the capacitive reactance of a string containing a capacitor unit with one (1) shorted element will be,

\[
X'_{STRING} = 2 \cdot \frac{15,920^2}{500,000} + XC'_{500} = 1,457.3 \Omega
\]

with the overall equivalent capacitive reactance of the upper bank \((C1)\) being,

\[
X'_{C1} = \frac{1}{\left[\frac{X_{STRING}}{3}\right]^{-1} + \left[X'_{STRING}\right]^{-1}} = 376.1 \Omega
\]

Since the three (3) low-voltage capacitors paralleled on the neutral end (see Figure 3.1) have such low reactance when compared to \(C_1\) and \(C_2\) they can be ignored. Their equivalent reactance is calculated as,

\[
X'_{CLV} = \frac{825^2}{3} = 1.36 \Omega
\]
The voltage across the upper stage can be calculated from voltage division assuming a nominal 161kV bus voltage,

\[ V'_{C1} = \frac{161,000}{\sqrt{3}} \frac{X'_{C1}}{X'_{C1} + X_{C2}} = 46,235.1\text{V} \]

The voltage across the capacitor unit with the shorted element can be calculated as,

\[ V'_{\text{CAN}} = V'_{C1} \cdot \frac{X'_{C500}}{X'_{C500} + 2 \cdot X'_{C500}} = 14,071.6\text{V} \]

and the voltage across each of the seven (7) remaining healthy elements in the capacitor unit with the shorted element will be,

\[ V'_{\text{ELEMENTS}} = \frac{V'_{\text{CAN}}}{7} = 2,010.2\text{V} \]

When compared to the rated voltage of each element (1,990V) we can see that only a slight overvoltage results from the shorting of one (1) element in one (1) capacitor unit in the upper bank (barely 1% over rated).

Referring to figures 2.2 and 3.2 we can apply voltage division to determine a generic formula to find the voltage \( V'_{E} \) across the remaining healthy elements in a capacitor unit with failed element(s). Let,

\[ V = \text{healthy phase to neutral bus voltage magnitude (volts)} \]

\[ S = \text{number of series groups in the bank that has the capacitor unit with failed elements} \]

\[ P = \text{number of parallel strings in the bank that has the capacitor unit with failed elements} \]

\[ E = \text{number of elements in series in one capacitor unit in the bank that has the capacitor unit with failed elements} \]

\[ F = \text{number of shorted elements in the capacitor unit with failed elements} \]

\[ N = \frac{(E-F)}{E} \]
$X_C =$ capacitive reactance of a single healthy capacitor unit in the bank that has the capacitor unit with failed elements

$X_{ELSE} =$ the total capacitive reactance of the rest of the capacitor bank

$\Lambda = \frac{X_C}{X_{ELSE}}$

For example, assuming there are two (2) elements shorted in a capacitor unit in the upper bank. In this case F equals two (2) and as such N will equal 6/8. Figure 3.3 shows the configuration and some of the variables needed for the calculation.

![Bank element detail](image)

Figure 3.3 Bank element detail

It is obvious from the upper bank in figure 3.3 that the equivalent reactance of the remaining healthy strings will be,
\[
\frac{S}{P-1} \cdot X_c = \frac{3}{4-1} \cdot X_c = 506.9\Omega
\]

The reactance of the faulty capacitor unit will be,

\[
N \cdot X_c = \frac{6}{8} \cdot X_c = 380.7\Omega
\]

The reactance of the rest of the series string containing the faulty capacitor will be,

\[
(S-1) \cdot X_c = (3-1) \cdot X_c = 1,013.8 \Omega
\]

The equivalent reactance of the bank with the faulty capacitor unit will be,

\[
X' = \frac{\frac{S}{P-1} \cdot (S-1+N) \cdot X_c}{\frac{S}{P-1} + (S-1+N)}
\]

The voltage across the upper capacitor bank when one capacitor unit has F shorted elements will be,

\[
V'_{BANK} = V \cdot \frac{\frac{S}{P-1} \cdot X_c \cdot (S-1+N) \cdot X_c}{\frac{S}{P-1} \cdot X_c + (S-1+N) \cdot X_c} = V \cdot \frac{\frac{S}{P-1} \cdot (S-1+N)}{\frac{S}{P-1} \cdot (S-1+N) + A \cdot \left( \frac{S}{P-1} + S-1+N \right)}
\]

Once the voltage across the bank containing the faulty capacitor unit has been found we can calculate the voltage across the faulty capacitor unit as,

\[
V'_{CAN} = V'_{BANK} \cdot \frac{N \cdot X_c}{(S-1+N) \cdot X_c} = V \cdot \frac{\frac{S}{P-1} \cdot N}{\frac{S}{P-1} \cdot (S-1+N) + A \cdot \left( \frac{S}{P-1} + S-1+N \right)}
\]
From which we can find the voltage across the remaining healthy elements inside the faulty capacitor unit as,

\[ V'_E = V \cdot \frac{S \cdot \frac{1}{E}}{P-1 \cdot \left( \frac{S}{P-1} \cdot (S-1+N) + \frac{S}{P-1} + S-1+ N \right)} \]

Using the above generic formula we can continue shorting elements in the faulty capacitor unit and populate Table 3.1 and Table 3.2.

Table 3.1
Healthy element voltage (faulty unit in upper bank)

<table>
<thead>
<tr>
<th>Number of shorted elements</th>
<th>Voltage on remaining elements in the capacitor unit</th>
<th>% voltage above rated (1,990V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2,009.8V</td>
<td>1.0%</td>
</tr>
<tr>
<td>2</td>
<td>2,088.8V</td>
<td>5.0%</td>
</tr>
<tr>
<td>3</td>
<td>2,174.3V</td>
<td>9.3%</td>
</tr>
<tr>
<td>4</td>
<td>2,267.2V</td>
<td>13.9%</td>
</tr>
<tr>
<td>5</td>
<td>2,368.2V</td>
<td>19.0%</td>
</tr>
<tr>
<td>6</td>
<td>2,478.8V</td>
<td>24.6%</td>
</tr>
</tbody>
</table>
Table 3.2
Healthy element voltage (faulty unit in lower bank)

<table>
<thead>
<tr>
<th>Number of shorted elements</th>
<th>Voltage on remaining elements in the capacitor unit</th>
<th>% voltage above rated (1,910V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>947.3</td>
<td>NA</td>
</tr>
<tr>
<td>5</td>
<td>1,025.7</td>
<td>NA</td>
</tr>
</tbody>
</table>

It is obvious that the lower bank will not experience overvoltages when the upper capacitor bank is in service (recall that it was energized at 48.7% of rated when both banks are in service). Shorted elements in the lower bank can stress the healthy elements in the upper bank as reflected in Table 3.3. However, it would require two entire series groups to be shorted out in one string of the lower bank.

Table 3.3
Healthy element voltage in upper bank (faulty unit in lower bank)

<table>
<thead>
<tr>
<th>Number of shorted elements</th>
<th>Voltage on remaining elements in the capacitor unit</th>
<th>% voltage above rated (1,990V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1,936.1V</td>
<td>NA</td>
</tr>
<tr>
<td>5</td>
<td>1,938.2V</td>
<td>NA</td>
</tr>
<tr>
<td>10 (entire unit)</td>
<td>1,962.0V</td>
<td>NA</td>
</tr>
<tr>
<td>20 (two entire units)</td>
<td>2,010.3V</td>
<td>1%</td>
</tr>
</tbody>
</table>
It is much more significant for the lower capacitor bank to experience shorted elements when the upper capacitor bank is bypassed resulting in full phase voltage being applied to the lower bank as can be seen in Table 3.4.

Table 3.4

Healthy element voltage in lower bank (faulty unit in lower bank/bypass closed)

<table>
<thead>
<tr>
<th>Number of shorted elements</th>
<th>Voltage on remaining elements in the capacitor unit</th>
<th>% voltage above rated (1,910V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1,851.9V</td>
<td>NA</td>
</tr>
<tr>
<td>1</td>
<td>1,889.2V</td>
<td>NA</td>
</tr>
<tr>
<td>2</td>
<td>1,927.9V</td>
<td>0.9%</td>
</tr>
<tr>
<td>3</td>
<td>1,970.4V</td>
<td>3.2%</td>
</tr>
<tr>
<td>4</td>
<td>2,032.2V</td>
<td>6.4%</td>
</tr>
<tr>
<td>5</td>
<td>2,057.0V</td>
<td>7.7%</td>
</tr>
<tr>
<td>6</td>
<td>2,104.9V</td>
<td>10.2%</td>
</tr>
</tbody>
</table>

Obviously the calculations to determine voltage differential set points for protection of the 2-stage capacitor bank are not trivial and involve two distinct configurations (upper bank bypassed or not bypassed) that require different setting groups for the protective relay depending on the state of the bypass switch (Figure 2.1). The remainder of the document describes a transient problem affecting the voltage differential protection as applied and a solution will be recommended that not only mitigates the transient problem, but also greatly simplifies the setting approach for the protection.
CHAPTER 4
TRANSIENT OPERATION

Bypass Closing

With the bypass switch closed to short the upper capacitor bank the operation of the bank is exactly the same as a traditional fuseless capacitor bank. The normal transients expected for capacitor bank operation (inrush, out-rush, back-to-back switching etc.) are no different for this configuration than for typical single-stage capacitor banks.

However, closing the bypass switch can produce a significant high-magnitude, high-frequency transient as the energy stored in the upper capacitor bank is released. To mitigate the damaging effects of this short-circuit event the bypass switch is equipped with an extra set of contacts fitted with 37.5Ω closing resistors that are momentarily in the circuit (e.g. 1 cycle) during the discharge. The total bank phase current is shown in Figure 4.1. This transient is within the range of normal bank switching transients.

Figure 4.1 Total bank phase current during bypass closing.
Bypass Opening

The opening of the bypass produces the transient of interest in this case and it presents a unique problem for the protection. When the bypass switch opens it interrupts current at a zero crossing. Since the voltage across and current through a reactive element are in quadrature the voltage will be at a peak. So, referring to Figure 4.2, it can be seen that both the lower capacitor bank \( C_2 \) and the low-voltage capacitance \( C_{LV} \) will both be experiencing peak voltage at the moment the bypass switch current goes through zero. However, the upper capacitor bank \( C_1 \) is discharged just prior to the bypass switch opening so it has no initial charge. This makes for an interesting transient as described below. First an analytical solution (closed form) will be developed and then verified with a transient analysis using ATP (Alternative Transients Program).

![Figure 4.2 Simplified one-line with VT detail.](image-url)
Analytical Development

The Laplace transform is an integral transform that is used to transform a function of time to a function of “s” where s is a complex argument. This allows us to solve a network problem using algebra and then apply the inverse transform to arrive at the various quantities of interest in the time domain. This procedure is followed below to calculate the various voltages of interest after the bypass switch is opened. Figure 4.3 shows the fundamental elements required and Figure 4.4 shows the transform pairs that will be useful in this exercise.

Figure 4.3 Fundamental element modeling in Laplace

\[
\begin{align*}
    f(t) &= \cos(\omega t) & F(s) &= \frac{\omega}{s^2 + \omega^2} \\
    f(t) &= \sin(\omega t) & F(s) &= \frac{s}{s^2 + \omega^2} \\
    f(t) &= 2Ae^{-\alpha t}\cos(\beta t + \theta) & F(s) &= \frac{A}{s + \alpha - j\beta} + \frac{A'}{s + \alpha + j\beta}
\end{align*}
\]

Note: \( \theta \) is the angle associated with the complex factor A

Figure 4.4 Useful Laplace transform pairs
The bus voltage will be at a peak when the bypass switch interrupts its current. As such we can use the cosine source (left in Figure 4.4) with a scale factor of $V_M$ where $V_M$ is the peak bus voltage or,

$$V_M = 161,000 \cdot \frac{\sqrt{2}}{\sqrt{3}} = 131,456\text{V}$$

and since $C_1 = C_2$ in this case we will just use $C$ to represent those values. Additionally, damping will be neglected but the inductance of the system equivalent will be added and it will have no initial energy value since the current when the bypass is opened will be zero. The resulting circuit is shown in Figure 4.5 where $C = 6.98\mu\text{F}$ and $C_{LV} = 1952\mu\text{F}$. Note that the upper capacitor bank is shorted prior to the bypass switch opening.

![Figure 4.5 Laplace network for solution (bypass switch shorted at t=0’)](image-url)

**Figure 4.5 Laplace network for solution (bypass switch shorted at t=0’)**
The initial voltage across the lower capacitor bank and across the low-voltage capacitance will be,

\[ V_C = V_M \cdot \frac{C_{LV}}{C + C_{LV}} = 0.996 \cdot V_M \]

\[ V_{CLV} = V_M \cdot \frac{C}{C + C_{LV}} = 0.03567 \cdot V_M \]

The resulting Laplace network with initial conditions is shown in Figure 4.6.

Figure 4.6 Laplace network with initial conditions for solution (t=0')

Applying simple network analysis techniques to the circuit we can find the current after the bypass switch opens as,
\[ I(s) = \frac{V_M s}{s^2 + 377^2} - \frac{V_M}{s} \left( \frac{2}{sC} + \frac{1}{sC_{LV}} \right) \]

which can be further simplified by substitution (where \( M \) calculates to 3200 radians/second) and manipulated into a form similar to the transform of \( \sin(Mt) \),

\[ M^2 = \frac{2}{LC} + \frac{1}{LC_{LV}} \]

\[ I(s) = \frac{V_M s^2 / L}{(s^2 + 377^2)(s^2 + M^2)} - \frac{V_M / L}{s^2 + M^2} \]

The closed form solution for the voltage waveform across the upper capacitor bank after the switch is opened can be found simply by multiplying the Laplace current, \( I(s) \), by the Laplace impedance of the upper capacitor bank, \( 1/sC \).

\[ V(s) = \frac{V_M s / CL}{(s^2 + 377^2)(s^2 + M^2)} - \frac{V_M M}{CLM} \]

Before this quantity can be inverse transformed into its time domain equivalent a partial fraction expansion is necessary (the asterisk denotes complex conjugate).

\[ \frac{V_M s / CL}{(s^2 + 377^2)(s^2 + M^2)} = \frac{A}{s - j377} + \frac{A^*}{s + j377} + \frac{B}{s - jM} + \frac{B^*}{s + jM} \]

with each expansion constant found as follows,
Now, expanding the second term from \( V(s) \),

\[
\begin{align*}
A &= \frac{V_M/\sqrt{\text{CL}}}{(s + j377)(s^2 + M^2)} \\
&= \frac{V_M/\sqrt{\text{CL}}}{2(-377^2 + M^2)} = 33306 \\
B &= \frac{V_M/\sqrt{\text{CL}}}{(s^2 + j377^2)(s + jM)} \\
&= \frac{V_M/\sqrt{\text{CL}}}{(-M^2 + j377^2)(2)} = -32840
\end{align*}
\]

Now, expanding the second term from \( V(s) \),

\[
\left[ \frac{V_M}{\sqrt{\text{CL}}M} \right] \frac{M}{s(s^2 + M^2)} = \frac{D}{s} + \frac{E}{s - jM} + \frac{E^*}{s + jM}
\]

\[
D = \left[ \frac{V_M}{\sqrt{\text{CL}}} \right] \frac{M}{M^2} = \frac{V_M/\sqrt{\text{CL}}}{M^2} = 65685 \\
\text{at } s = 0
\]

\[
E = \frac{V_M/\sqrt{\text{CL}}}{s(s + jM)} = \frac{V_M/\sqrt{\text{CL}}}{jM(2jM)} = \frac{-V_M/\sqrt{\text{CL}}}{2M^2} = -32840 \\
\text{at } s = jM
\]
and finally we have the Laplace function for the voltage $V(s)$ across the upper capacitor bank after the bypass switch is opened,

$$V(s) = \frac{A}{(s - j377)} + \frac{A^*}{(s + j377)} + \frac{B}{(s - jM)} + \frac{B^*}{(s + jM)} - \frac{D}{s} - \frac{E}{(s - jM)} - \frac{E^*}{(s + jM)}$$

where $A = 33306$, $B = -32840$, $D = 65685$, and $E = -32840$. It can be seen that the “B” and “E” terms will cancel and then the inverse transformed time domain voltage will be,

$$V(t) = 2|33306|\cos(377t) - 65685$$

which can be further simplified to,

$$V(t) = 66612\cos(377t) - 65685$$

This voltage will oscillate between zero and 130,370V. The capacitor units in the upper bank are rated 15.92kV with three (3) in series for a bank rated RMS voltage of 47.76kV. The RMS voltage can be calculated simply as,

$$V(t)_{\text{rms}} = \sqrt{\left(\frac{66612}{\sqrt{2}}\right)^2 + 65685^2} \approx 80.8kV$$

which is an RMS overvoltage of 1.69 per unit. The large dc component will discharge slowly across the 8.56MΩ discharge resistors (built into each individual capacitor unit). This RMS voltage decay can be compared to the short time overvoltage power frequency capability of the capacitor units [7] given in Figure 4.7.
Figure 4.7 Short time overvoltage capability

A comparison of the upper capacitor bank RMS voltage profile (from simulation) against Figure 4.8 shows that the application is likely acceptable although it is prudent to obtain manufacturer concurrence.
Figure 4.8 Simulation results against standard capability

The voltage across the lower capacitor bank can be found in a similar fashion and it will have an additional term due to the initial voltage across that capacitance.

\[
V(t) = 66612\cos(377t) - 65685 + 0.996V_m
\]

This voltage will oscillate between zero and 128,240V.

Figure 4.9 shows the voltage across the upper capacitor bank and the voltage across the lower capacitor bank. Note that the voltages are both completely offset by their respective dc component. It is this dc voltage that hinders the voltage differential protection as will be subsequently explained.
Figure 4.9 Voltage across upper and lower capacitor banks after bypass opened

Following a similar approach the closed form solution for the voltage across the low-voltage capacitors can be found. This is of critical importance as this is the voltage that is presented to the VT measuring the tap point voltage for the voltage differential protection. It is this dc component that saturates the VT defeating the ability of the voltage differential protection to function properly.

\[
V_{LV}(s) = \frac{V_M s}{(s^2 + 377^2)(s^2 + M^2)} - \frac{V_M M}{C_{LV} s (s^2 + M^2)} + \frac{C}{s(C + C_{LV})} V_M
\]

\[
V(t) = 228 \cos(377t) + 234
\]

This voltage from simulation is shown in Figure 4.10 which agrees nicely with the closed form solution above. The full dc offset is evident.
Simulations (effect on protection)

As discussed above, the primary capacitor bank protection is the voltage differential function that compares the bus voltage to the tap voltage on a per-phase basis as,

$$\Delta V = V_x - kV_Y$$

however, when the large dc offset occurs in the tap point voltage (note that the bus voltage does not experience a dc offset) the tap point VT experiences saturation which will be shown with simulation results as well as captured oscillography from the actual installation.

The simulation model was constructed in ATPDraw version 5.8 and cases executed using ATP. Figure 4.11 shows the simplified model. The upper and lower capacitor banks are each modeled as a single lumped capacitance with a single lumped resistance in parallel representing their discharge resistance.

Figure 4.10 Voltage at the tap point (across low-voltage capacitance) after bypass opened
A more detailed model is used when studying the overvoltages due to shorted capacitor elements, but it is not needed when studying the effects of bypass opening. The 37.5Ω closing resistor is modeled in series with a small stray inductance both of which are in parallel with the main contacts which close one (1) cycle after the resistor contacts. In series with this combination is stray resistance and inductance through the connection to the top of the lower capacitor bank. At the neutral the three (3) low-voltage capacitors in parallel are modeled as a single lumped 1952μF capacitance with the equivalent discharge resistance in parallel. From the tap point a 100Ω ferroresonance suppression resistor [6] is in series with the 3.2 to 1 ratio VT.

Figure 4.11 Simulated network (A-phase only)
Figure 4.12 below is captured oscillographic data showing the tap point VT secondary voltage as recorded by a digital fault recorder when the bypass switch was opened on the actual installation. It compares very well to the voltage as computed in the ATP simulation (Figure 4.13).

![Figure 4.12 Captured voltage on the VT secondary when bypass switch opened](image)

![Figure 4.13 Simulated voltage on the VT secondary when bypass switch opened](image)

The saturation of the VT results in a false differential voltage and a subsequent misoperation of the voltage differential protection. Note that the dc offset in and of itself is not a problem for modern digital protection relays since their analog and digital filtering removes it from the operate quantities. The dc offset is a problem because it saturates the tap point VT with a subsequent reduction in the fundamental frequency component measured.

The false differential voltage will be present until the dc offset in the low-voltage capacitors has decayed and the VT has come out of saturation. This decay (Figure 4.14) is a simple RC decay through the discharge resistors in the capacitor units. To prevent misoperation
of the sensitive voltage differential the protection must be disabled for several seconds which is undesirable.

Figure 4.14 Simulated voltage across low-voltage capacitors with RMS value

Simulations (mitigations)

650μF Series Capacitor

One possible solution is to put a capacitor in series with the 100Ω resistor and VT to filter the dc to the VT. This met with some success and eliminated the VT saturation in around 10 cycles but it did not eliminate the problem. As such, the voltage differential protection would still need to be disabled briefly.
Remove the 100Ω resistor

The dc offset across the low-voltage capacitors decays much faster than the dc offset across the upper and lower capacitor banks. This is because when the VT saturates it places the 100Ω resistor in series with a relatively low magnetizing inductance of the VT and its primary winding resistance of 20Ω allowing a low impedance path for the dc voltage to decay through as compared to the high resistance of the equivalent discharge resistance of the low-voltage capacitors (approximately 103kΩ). However, it does take time for this dc to decay through the 100Ω resistor. If this resistor can be removed from the circuit the decay would occur faster as shown in Figure 4.16. However, similar to the 650μF series capacitor case, it still takes time for the decay and the voltage differential would have to be disabled for that period. Further, removing the 100Ω resistor would have to be studied in detail as it is purportedly inserted for ferroresonance suppression [6].
Reconfigure the VT

In the 2012 revision of [6] a new section was added (8.3.6.4) describing a modification to the traditional voltage differential protection for a split wye grounded fuseless capacitor bank. In this configuration (Figure 4.17) the individual phase is split into two halves and a VT is inserted above the low-voltage capacitors. This allows sensitive voltage differential protection to be achieved with a single voltage (doesn’t require comparison with the bus voltage).

Furthermore, it provides a complete and satisfactory solution to the dc offset concern. Since both low-voltage capacitances would experience the same dc offset the voltage presented to the VT would only experience parasitic levels of dc due to equipment tolerances.
The present limitation in implementing this scheme is that traditional (including modern digital relays) voltage differential protection works based on the equation,

$$\Delta V = V_X - kV_Y$$

which requires the bus voltage and tap voltage to be measured and compared. A very important feature of modern relays is the ability to “null” this differential voltage after the capacitor bank has been placed in service. However, no modern digital relay has built in logic to accommodate the “nulling” if only one voltage is presented to the relay. With present relays the nulling would have to be done manually and would simply require the user poll the relay for the measured voltage which would then be used to offset (positive or negative depending on measured sign) the overvoltage set points calculated for the alarm and trip thresholds.

The existing simulation configuration was changed to the “split-wye” configuration as shown in Figure 4.17 and the simulation results shown in Figure 4.18 show that this would be an
optimum solution as the voltage across the VT is undisturbed during the operation of the bypass switch.

Figure 4.18 Left and Right low-voltage capacitor voltages and their difference
CHAPTER 5
CONCLUSIONS

The two-stage capacitor bank is an application of shunt capacitors with many advantages and one major feature of operation (dc offset on bypass opening) that poses a major challenge to voltage differential protection. This paper has provided a detailed explanation of voltage differential protection of shunt capacitor banks including specifics on how to calculate set points for the two-stage capacitor bank. Then the major challenge was addressed with closed form analysis and transient simulation with an EMTP program. Various mitigations were suggested and studied with an optimum solution being presented last. This solution is the superior solution for the following reasons.

- It results in the sensitive voltage differential being operational 100% of the time
- Disabling protection during switching is not required
- No need to have different voltage differential settings for the two bank configurations
- No need to install the 100Ω ferroresonance suppression resistor

It is hoped that this work will provide a worthwhile improvement in the state-of-art of protection of these specialized shunt capacitor banks resulting in improved system reliability and protection of critical assets.
REFERENCES


VITA

Russell William Patterson was born in Tupelo, Mississippi, on June 7, 1967, the son of Donna June Patterson and John William Patterson. After completing his degree at Tupelo High School, Tupelo, Mississippi, in 1985 he enrolled in Itawamba Community College in Tupelo, receiving an Associates of Applied Science degree in Robotics and Automated Systems in 1987, after which he began pursuing a Bachelor’s of Science in Electrical Engineering, receiving his degree in 1991 from Mississippi State University in Starkville, Mississippi.

After graduating from Mississippi State University he joined the Tennessee Valley Authority (TVA) as a field engineer in the West Point, Mississippi field office. In 1993 he joined the staff of the System Protection & Analysis department in Chattanooga, Tennessee where he eventually became manager of the department.

In the fall of 2008 Russell left the TVA to begin a career as power system consultant specializing in system protection. In May of 2010 he opened Patterson Power Engineers, LLC located in Chattanooga, Tennessee which presently employs seven full time engineers. He has authored or co-authored many papers on power system protection and analysis and is Chairman of the Line Protection Subcommittee of the IEEE Power System Relaying Committee.